CLAIMS

I claim:

1. A dielectric spacer structure, comprising:

a first oxide layer deposited over a top surface of a wafer and abutting a gate structure;

a silicon-nitride barrier layer deposited over said first oxide layer, wherein said silicon-nitride barrier layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces, thereby enabling formation of said silicon nitride barrier layer without nitridizing said first oxide layer; and

a second oxide layer formed over said silicon-nitride barrier layer.

2. The dielectric spacer structure of claim 1, further comprising an etch stop nitride layer formed between said silicon-nitride barrier layer and said second oxide layer, wherein said etch stop nitride layer is formed through a process that includes ammonium precursors.

3. The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through an atomic layer deposition process.

4. The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through an atomic layer deposition of silicon that is nitridized by a plasma process.

5. The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through vapor deposition of a nitrogen-silicon gas containing a non-ammonia based organic precursor.

6. The dielectric spacer structure of claim 1, wherein said silicon-nitride barrier layer is formed from vapor deposition of N_2 and $SiCl_4$.

7. The dielectric spacer structure of claim 1, wherein said silicon-nitride barrier layer is formed from vapor deposition of N_2 and SiF_4.

8. The dielectric spacer structure of claim 2, wherein said silicon-nitride barrier layer has a thickness of 1.5 to 3.0 nm and said etch stop nitride layer has a thickness of 30 nm to 90 nm.

9. The dielectric spacer structure of claim 3, wherein said silicon-nitride barrier layer has a thickness of 30 nm to 90 nm.

10. A spacer, comprising:

a first spacer oxide layer abutting a gate structure of a MOSFET;

a silicon-nitride layer formed over said first spacer oxide layer, wherein said silicon-nitride layer includes barrier means to inhibit ammonium precursors from reaching and interacting with said first spacer oxide layer, thereby protecting said first spacer oxide layer from nitridization by said ammonium precursors; and

a second spacer oxide layer formed over said silicon nitride layer.

11. The spacer of claim 10, wherein said barrier means is formed through deposition means that create a nitride barrier layer without nitridizing said first spacer oxide layer.

12. The spacer of claim 10, wherein said barrier means is formed from a layer of nitridized silicon.

13. The spacer of claim 10, wherein said silicon-nitride layer has a thickness of 30 nm to 90 nm, wherein 1.5 nm to 3.0 nm of said silicon-nitride layer forms said barrier means.

14. The dielectric spacer structure of claim 10, wherein said barrier means blocks diffusion of ammonium precursors into said first spacer oxide layer.

15. A spacer stack, comprising:

a first oxide spacer layer free of nitridization that abuts a MOSFET gate electrode;

a silicon-nitride layer formed over said dielectric layer; and

a second oxide spacer layer formed over said silicon-nitride layer.

16. The spacer stack of claim 15, wherein said spacer structure includes a barrier layer formed between said silicon-nitride layer and said first oxide spacer layer.

17. The spacer stack of claim 16, wherein said barrier layer is formed of silicon-nitride having a thickness of 1.5 nm to 3.0 nm.

18. The spacer stack of claim 17, wherein said barrier layer is formed through atomic layer deposition.

19. The spacer stack of claim 17, wherein said barrier layer is formed through vapor deposition of silicon-nitride.

20. The spacer stack of claim 17, wherein said barrier layer is formed through nitridization of a silicon layer that is deposited between said silicon-nitride layer and said first spacer oxide layer.